

Am29LV008T/Am29LV008B

8 Megabit (1,048,576 x 8-Bit) CMOS 3.0 Volt-only,
Sectored Flash Memory

DISTINCTIVE CHARACTERISTICS

■ Single power supply operation

- Extended voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- Standard voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors

■ High performance

- Extended voltage range: access times as fast as 100 ns
- Standard voltage range: access times as fast as 90 ns

■ Ultra low power consumption

- Automatic Sleep Mode: 200 nA typical
- Standby mode: 200 nA typical
- Read mode: 2 mA/MHz typical
- Program/erase mode: 20 mA typical

■ Flexible sector architecture

- One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbyte sectors
- Supports control code and data storage on a single device
- Sector Protection features:
 - A hardware method of locking a sector to prevent any program or erase operations within that sector
 - Temporary Sector Unprotect feature allows code changes in previously locked sectors

■ Top or bottom boot block configurations available

■ Embedded Algorithms

- Embedded Erase algorithms automatically preprogram and erase the entire chip or any combination of designated sectors
- Embedded Program algorithms automatically write and verify bytes or words at specified addresses

■ Minimum 100,000 write cycle guarantee per sector

■ Package option

- 40-pin TSOP

■ Compatibility with JEDEC standards

- Pinout and software compatible with single-power supply Flash
- Superior inadvertent write protection

■ Data Polling and toggle bits

- Provides a software method of detecting program or erase operation completion

■ Ready/Busy pin

- Provides a hardware method of detecting program or erase cycle completion

■ Erase suspend/resume feature

- Provides the ability to suspend the erase operation in any sector, read data from or program data to any other sector, then return to the original sector and complete the initial erase operation

■ Hardware reset pin ($\overline{\text{RESET}}$)

- Hardware method to reset the device to the read mode

GENERAL DESCRIPTION

The Am29LV008 is an 8 Mbit, 3.0 Volt-only Flash memory organized as 512 Kbytes of 8 bits each. For flexible erase and program capability, the 512 Kbits of data is divided into 19 sectors of one 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbytes. The data appears on DQ0–DQ7. The Am29LV008 is offered in a 40-pin TSOP package. This device is designed to be pro-

grammed in-system with the standard system 3.0 volt V_{CC} supply. The device can also be reprogrammed in standard EPROM programmers.

The Am29LV008 provides two levels of performance. The first level offers access times as fast as 100 ns with a V_{CC} range as low as 2.7 volts, which is optimal for battery powered applications. The second level offers a

90 ns access time, optimizing performance in systems where the power supply is in the regulated range of 3.0 to 3.6 volts. To eliminate bus contention, the device has separate chip enable (\overline{CE}), write enable (\overline{WE}), and output enable (\overline{OE}) controls.

The Am29LV008 is entirely command set-compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The Am29LV008 is programmed by executing the program command sequence. This invokes the Embedded Program Algorithm, which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The device is erased by executing the erase command sequence. This invokes the Embedded Erase Algorithm, which is an internal algorithm that automatically preprograms the array, if it is not already programmed, before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture. This allows for sectors of memory to be erased and reprogrammed without affecting the data contents of other sectors. A sector is typically erased and verified within 1.0 second. The Am29LV008 is fully erased when shipped from the factory.

The Am29LV008 device also features hardware sector protection, implemented via external programming equipment, which disables both program and erase operations in any combination of the memory sectors.

The Erase Suspend feature enables the user to pause the erase operation, for any period of time, to read data from or program data to a sector that was not being erased. Thus, true background erase can be achieved.

The device features 3.0 volt, single-power-supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by the $\overline{RY}/\overline{BY}$ pin. \overline{Data} Polling of DQ7, or by the Toggle Bit (DQ6). Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

The Am29LV008 also has a hardware \overline{RESET} pin. When this pin is driven low, execution of any Embedded Program or Erase Algorithm will be terminated. The internal state machine is then be reset into the read mode. Resetting the device will enable the system's microprocessor to read the boot-up firmware from the Flash memory.

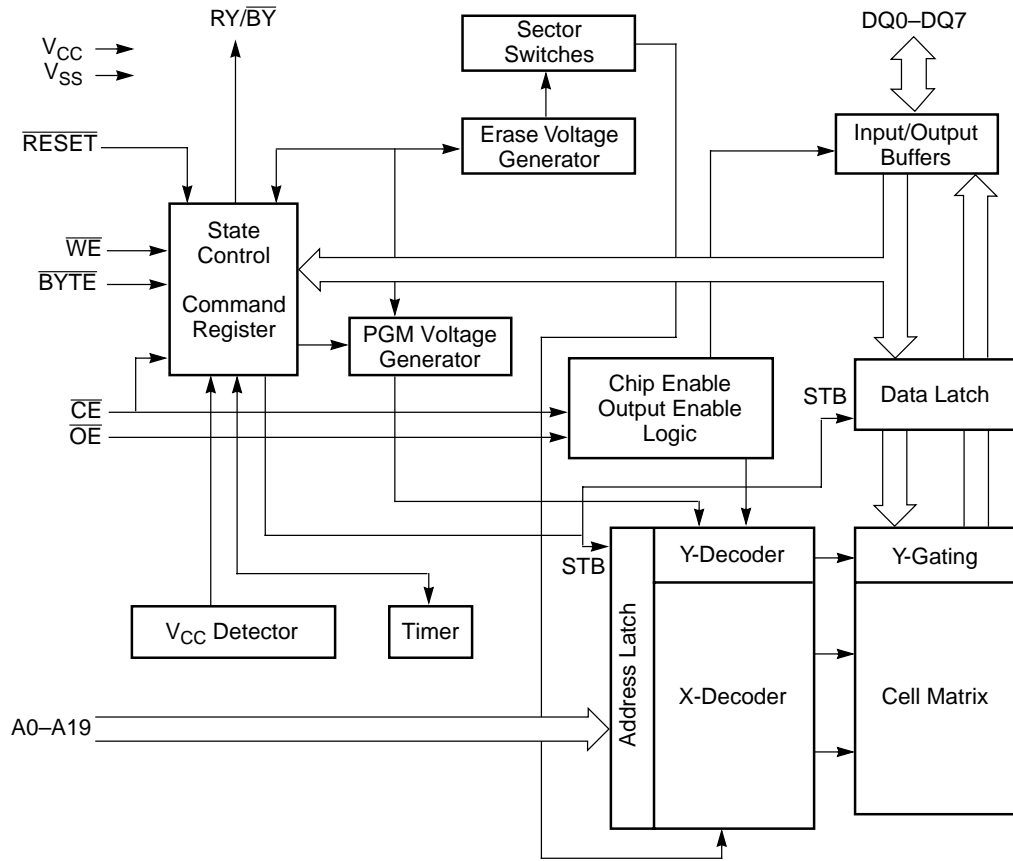
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29LV008 memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

PRODUCT SELECTOR GUIDE

Family Part Number	Am29LV008T/Am29LV008B			
Ordering Part Number: $V_{CC} = 3.0\text{--}3.6\text{ V}$	-90R			
$V_{CC} = 2.7\text{--}3.6\text{ V}$		-100	-120	-150
Max access time (ns)	90	100	120	150
\overline{CE} access time (ns)	90	100	120	150
\overline{OE} access time (ns)	40	40	50	55

3.0 V-only Flash

BLOCK DIAGRAM

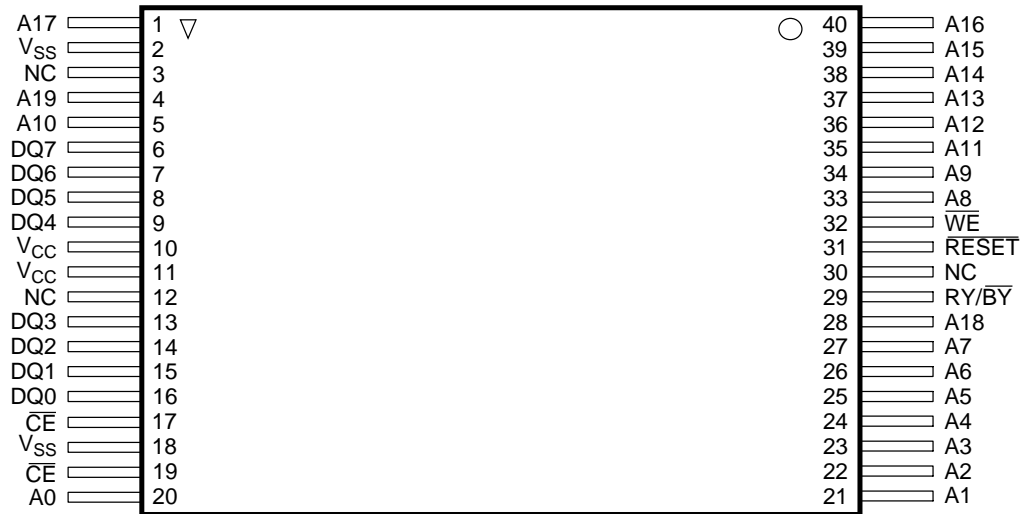


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CONNECTION DIAGRAMS



Standard 40-Pin TSOP



Reverse 40-Pin TSOP

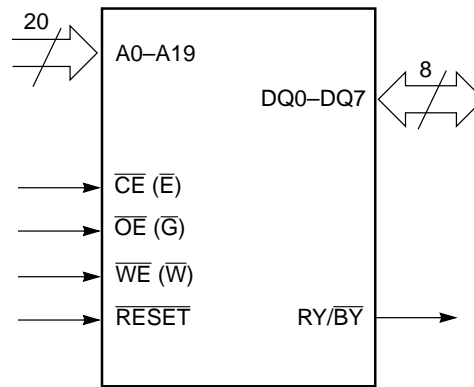
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PIN CONFIGURATION

- A0–A19 = 20 addresses
- DQ0–DQ7 = 8 data inputs/outputs
- \overline{CE} = Chip enable
- \overline{OE} = Output enable
- \overline{WE} = Write enable
- \overline{RESET} = Hardware reset pin, active low
- RY/\overline{BY} = Ready/ \overline{Busy} output
- V_{CC} = Standard voltage range
(3.0 V to 3.6 V) for -90R

Extended voltage range
(2.7 to 3.6 V) for -100, -120, -150
- V_{SS} = Device ground
- NC = Pin not connected internally

LOGIC SYMBOL



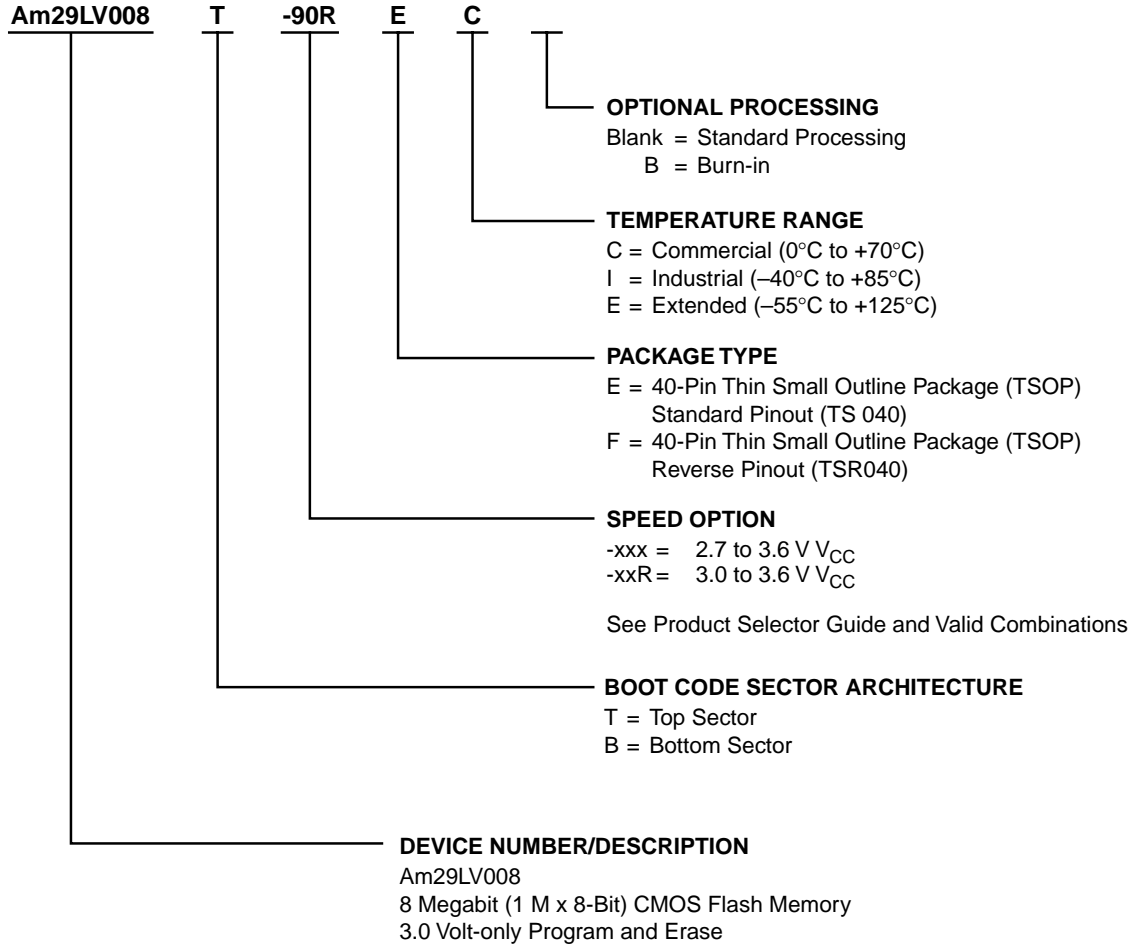
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3.0 V-only Flash

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am29LV008T-90R, Am29LV008B-90R $V_{CC} = 3.0-3.6 V$	EC, EI, FC, FI
Am29LV008T-100, Am29LV008B-100	EC, EI, EE, EEB, FC, FI, FE, FEB
Am29LV008T-120, Am29LV008B-120	
Am29LV008T-150, Am29LV008B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1. Am29LV008 User Bus Operations

Operation	\overline{CE}	\overline{OE}	\overline{WE}	A0	A1	A6	A9	DQ0–DQ7	\overline{RESET}
Autoselect, Manufacturer Code (Note 1)	L	L	H	L	L	L	V_{ID}	Code	H
Autoselect, Device Code (Note 1)	L	L	H	H	L	L	V_{ID}	Code	H
Read	L	L	H	A0	A1	A6	A9	RD	H
Standby	H	X	X	X	X	X	X	HIGH Z	H
Output Disable	L	H	H	X	X	X	X	HIGH Z	H
Write	L	H	L	A0	A1	A6	A9	PD (Note 2)	H
Enable Sector Protect (Note 3)	L	V_{ID}	Pulse/H	L	H	L	V_{ID}	Code	H
Verify Sector Protect (Note 4)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V_{ID}
Reset	X	X	X	X	X	X	X	HIGH Z	L

Legend:

L = V_{IL} , H = V_{IH} , V_{ID} = 12.0 V \pm 5%, X = Don't care. See "DC Characteristics" on page 26 for voltage levels.

PD = program data, RD = read data. Refer to Table 3 on page 10 for more information.

Notes:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 5 on page 13.
2. Refer to Table 5 for valid PD during a write operation.
3. Set V_{CC} = 3.0 volts \pm 10%.
4. Refer to "Sector Protection" on page 12.

USER BUS OPERATIONS

Read Mode

The Am29LV008 has three control functions which must be satisfied in order to obtain data at the outputs:

- \overline{CE} is the power control and should be used for device selection ($\overline{CE} = V_{IL}$)
- \overline{OE} is the output control and should be used to gate data to the output pins if the device is selected ($\overline{OE} = V_{IL}$)
- \overline{WE} remains at V_{IH}

Address access time (T_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (T_{CE}) is the delay from stable addresses and stable \overline{CE} to valid data at the output pins. The output enable access time (T_{OE}) is the delay from the falling edge of \overline{OE} to valid data at the output pins (assuming the addresses have been stable at least $T_{ACC} - T_{OE}$ time).

Standby Mode

The Am29LV008 is designed to accommodate low standby power consumption by applying the following voltages to the \overline{CE} and \overline{RESET} pins: I_{CC3} for CMOS compatible I/Os (current consumption $<5 \mu A$ max.) is enabled when a CMOS logic level '1' ($V_{CC} \pm 0.3 V$) is applied to the \overline{CE} control pin with $\overline{RESET} = V_{CC} \pm 0.3 V$. While in the I_{CC3} standby mode, the data I/O pins remain in the high impedance state independent of the voltage level applied to the \overline{OE} input. See the DC Characteristics section for more details on Standby Modes.

Deselecting \overline{CE} (\overline{CE} and $\overline{RESET} = V_{CC} \pm 0.3 V$) puts the device into the I_{CC3} standby mode. If the device is deselected during an Embedded Algorithm operation, it continues to draw active power (I_{CC2}) prior to entering the standby mode, until the operation is complete. When the device is again selected ($\overline{CE} = V_{IL}$), active operations occur in accordance with the AC timing specifications.

Automatic Sleep Mode

Advanced power management features such as the automatic sleep mode minimize Flash device energy consumption. This is extremely important in battery-powered applications. The Am29LV008 automatically enables the low-power, automatic sleep mode when addresses remain stable for 200 ns. Automatic sleep mode is independent of the \overline{CE} , \overline{WE} , and \overline{OE} control signals. Typical sleep mode current draw is 200 nA (for CMOS-compatible operation). Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

Output Disable

If the \overline{OE} input is at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The Autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. The intent is to allow programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The Autoselect command may also be used to check the status of write-protected sectors (see Table 2). This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} ($12.0\text{ V} \pm 5\%$) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH} . All addresses are don't cares except A0, A1, and A6 see Table 2.

The manufacturer and device codes may also be read via the command register, for instances when the

Am29LV008 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 5 on page 13.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer's code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the Am29LV008 these two bytes are given in Table 2. All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing Autoselect, A1 must be V_{IL} (see Table 2). The device code is 3EH (for top boot block) or 37H (for bottom boot block).

In order to determine which sectors are write protected, A1 must be at V_{IH} while running through the sector addresses; if the selected sector is protected, a logical '1' will be output on DQ0 ($DQ0 = 1$).

Table 2. Autoselect/Sector Protection Codes

Type	A13–A19	A6	A1	A0	Code (HEX)	DQ 7	DQ 6	DQ 5	DQ 4	DQ 3	DQ 2	DQ 1	DQ 0
Manufacturer Code: AMD	X	L	L	L	01H	0	0	0	0	0	0	0	1
29LV008 Device (Top Boot Block)	X	L	L	H	3EH	0	0	1	1	1	1	1	0
29LV008 Device (Bottom Boot Block)	X	L	L	H	37H	0	0	1	1	0	1	1	1
Sector Protection	Set Sector Addresses	L	H	L	01H*	0	0	0	0	0	0	0	1

X = Don't care.

* Outputs 01H at protected sector addresses.

Table 3. Sector Address Tables (Am29LV008T)

	A19	A18	A17	A16	A15	A14	A13	Sector Size	Address Range
SA0	0	0	0	0	X	X	X	64 Kbytes	0000h-0FFFFh
SA1	0	0	0	1	X	X	X	64 Kbytes	1000h-1FFFFh
SA2	0	0	1	0	X	X	X	64 Kbytes	2000h-2FFFFh
SA3	0	0	1	1	X	X	X	64 Kbytes	3000h-3FFFFh
SA4	0	1	0	0	X	X	X	64 Kbytes	4000h-4FFFFh
SA5	0	1	0	1	X	X	X	64 Kbytes	5000h-5FFFFh
SA6	0	1	1	0	X	X	X	64 Kbytes	6000h-6FFFFh
SA7	0	1	1	1	X	X	X	64 Kbytes	7000h-7FFFFh
SA8	1	0	0	0	X	X	X	64 Kbytes	8000h-8FFFFh
SA9	1	0	0	1	X	X	X	64 Kbytes	9000h-9FFFFh
SA10	1	0	1	0	X	X	X	64 Kbytes	A000h-AFFFFh
SA11	1	0	1	1	X	X	X	64 Kbytes	B000h-BFFFFh
SA12	1	1	0	0	X	X	X	64 Kbytes	C000h-CFFFFh
SA13	1	1	0	1	X	X	X	64 Kbytes	D000h-DFFFFh
SA14	1	1	1	0	X	X	X	64 Kbytes	E000h-EFFFFh
SA15	1	1	1	1	0	X	X	32 Kbytes	F000h-F7FFFh
SA16	1	1	1	1	1	0	0	8 Kbytes	F800h-F9FFFh
SA17	1	1	1	1	1	0	1	8 Kbytes	FA00h-FBFFFh
SA18	1	1	1	1	1	1	X	16 Kbytes	FC00h-FFFFh

Table 4. Sector Address Tables (Am29LV008B)

	A19	A18	A17	A16	A15	A14	A13	Sector Size	Address Range
SA0	0	0	0	0	0	0	X	16 Kbytes	0000h-03FFFh
SA1	0	0	0	0	0	1	0	8 Kbytes	0400h-05FFFh
SA2	0	0	0	0	0	1	1	8 Kbytes	0600h-07FFFh
SA3	0	0	0	0	1	X	X	32 Kbytes	0800h-0FFFFh
SA4	0	0	0	1	X	X	X	64 Kbytes	1000h-1FFFFh
SA5	0	0	1	0	X	X	X	64 Kbytes	2000h-2FFFFh
SA6	0	0	1	1	X	X	X	64 Kbytes	3000h-3FFFFh
SA7	0	1	0	0	X	X	X	64 Kbytes	4000h-4FFFFh
SA8	0	1	0	1	X	X	X	64 Kbytes	5000h-5FFFFh
SA9	0	1	1	0	X	X	X	64 Kbytes	6000h-6FFFFh
SA10	0	1	1	1	X	X	X	64 Kbytes	7000h-7FFFFh
SA11	1	0	0	0	X	X	X	64 Kbytes	8000h-8FFFFh
SA12	1	0	0	1	X	X	X	64 Kbytes	9000h-9FFFFh
SA13	1	0	1	0	X	X	X	64 Kbytes	A000h-AFFFFh
SA14	1	0	1	1	X	X	X	64 Kbytes	B000h-BFFFFh
SA15	1	1	0	0	X	X	X	64 Kbytes	C000h-CFFFFh
SA16	1	1	0	1	X	X	X	64 Kbytes	D000h-DFFFFh
SA17	1	1	1	0	X	X	X	64 Kbytes	E000h-EFFFFh
SA18	1	1	1	1	X	X	X	64 Kbytes	F000h-FFFFh

Write

Device erasure and programming are accomplished via the command register. The command register is written by bringing \overline{WE} to V_{IL} , while \overline{CE} is at V_{IL} and \overline{OE} is at V_{IH} . Addresses are latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs later, while data is latched on the rising edge of the \overline{CE} or \overline{WE} pulse, whichever occurs first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

Sectors of the Am29LV008 may be hardware protected at the user's factory with external programming equipment. The protection circuitry will disable both program and erase functions for the protected sectors, making the protected sectors read-only. Requests to program or erase a protected sector will be ignored by the device. If the user attempts to write to a protected sector, \overline{DATA} Polling will be activated for about 1 μ s; the device will then return to read mode, with data from the protected sector unchanged. If the user attempts to erase a protected sector, Toggle Bit will be activated for about 50 μ s; the device will then return to read mode, without having erased the protected sector.

It is possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order address A18–A12 represents the sector address, will produce a logical '1' at DQ0 for a protected sector.

Temporary Sector Unprotect

The sectors of the Am29LV008 may be temporarily unprotected by raising the \overline{RESET} pin to 12.0 volts (V_{ID}). During this mode, formerly protected sectors can be programmed or erased with standard command sequences by selecting the appropriate byte or sector addresses. Once the \overline{RESET} pin goes to V_{IH} , all the previously protected sectors will be protected again.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register.

Writing incorrect address and data values or writ-

ing them in the improper sequence will reset the device to the read mode. Table 5 on page 13 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

Read/Reset Command

The device will automatically power up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Characteristics section for the specific timing parameters.

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. The Am29LV008 contains an autoselect command operation that provides device information and sector protection status to the system. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacturer code of 01H. A read cycle from address XX01H returns the device code 3EH (for top boot device) or 37H (for bottom boot device); see Table 2 on page 9. All manufacturer and device codes will exhibit odd parity with the MSB of the lower byte (DQ7) defined as the parity bit. Scanning the sector addresses (A13, A14, A15, A16, A17, A18, and A19) while (A6, A1, A0) = (0, 1, 0) will produce a logical '1' code at device output DQ0 for a write protected sector (See Table 2).

To terminate the Autoselect operation, it is necessary to write the read/reset command sequence into the register.

Table 5. Am29LV008 Command Definitions

Command Sequence Read/Reset (Note 2)	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Read/Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset/Read	1	XXX	F0	RA	RD								
Autoselect Manufacturer ID	3	555	AA	2AA	55	555	90	X00	01				
Autoselect Device ID (Top Boot Block)	3	555	AA	2AA	55	555	90	X01	3E				
Autoselect Device ID (Bottom Boot Block)	3	555	AA	2AA	55	555	90	X01	37				
Autoselect Sector Protect Verify (Note 3)	3	555	AA	2AA	55	555	90	SA X02	00				
									01				
Byte Program	4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 4)	1	XXX	B0										
Erase Resume (Note 5)	1	XXX	30										

Legend:

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the \overline{WE} or \overline{CE} pulse.

PD = Data to be programmed at location PA. Data is latched on the rising edge of \overline{WE} or \overline{CE} pulse.

SA = Address of the sector to be erased or verified. Address bits A19–A13 uniquely select any sector.

Notes:

- All values are in hexadecimal.
- See Table 1 for description of bus operations.
- The data is 00h for an unprotected sector and 01h for a protected sector. The complete bus address is composed of the sector address on A19–A13 and 02h on A7–A0.
- Read and program functions in non-erasing sectors are allowed in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
- The Erase Resume command is valid only during the Erase Suspend mode.
- Unless otherwise noted, address bits A19–A11 = X = don't care.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. There are two “unlock” write cycles. These are followed by the program command and address/data write cycles. Addresses are latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs later, while the data is latched on the rising edge of \overline{CE} or \overline{WE} , whichever occurs first. The rising edge of \overline{CE} or \overline{WE} , whichever occurs first, initiates programming using the Em-

bedded Program Algorithm. Upon executing the write command, the system is **not** required to provide further controls or timing. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The status of the Embedded Program Algorithm operation can be determined three ways:

- \overline{DATA} Polling of DQ7

- Checking the status of the toggle bit DQ6
- Checking the status of the RY/ $\overline{\text{BY}}$ pin

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during a programming operation, the data at that location will be corrupted.

Programming is allowed in any sequence and across sector boundaries. Beware that a data '0' cannot be programmed back to a '1'. Attempting to do so will cause the device to exceed programming time limits ($\text{DQ5} = 1$) or result in an apparent success according to the data polling algorithm. However, reading the device after executing the Read/Reset operation will show that the data is still '0'. Only erase operations can convert '0's to '1's.

Figure 4 illustrates the Embedded Program Algorithm, using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles, followed by writing the erase "set up" command. Two more "unlock" write cycles are followed by the chip erase command.

Chip erase does **not** require the user to preprogram the device to all '0's prior to erase. Upon executing the Embedded Erase Algorithm command sequence, the device automatically programs and verifies the entire memory to an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The Embedded Erase Algorithm erase begins on the rising edge of the last $\overline{\text{WE}}$ or $\overline{\text{CE}}$ (whichever occurs first) pulse in the command sequence. The status of the Embedded Erase Algorithm operation can be determined three ways:

- $\overline{\text{DATA}}$ Polling of DQ7
- Checking the status of the toggle bit DQ6
- Checking the status of the RY/ $\overline{\text{BY}}$ pin

Figure 5 illustrates the Embedded Erase Algorithm, using a typical command sequence and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" writes. These are followed by writing the erase "set up" command. Two more "unlock" writes are followed by the Sector Erase command (30H). The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ (whichever occurs last) while the command (30H) is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ (whichever occurs first).

Multiple sectors can be specified for erase by writing the six bus cycle operation as described above and

then following it by additional writes of the Sector Erase command to addresses of other sectors to be erased. The time between Sector Erase command writes must be less than 80 μs , otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 μs from the rising edge of the last $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) occurs within the 80 μs time-out window, the timer is reset. During the 80 μs window, any command other than Sector Erase or Erase Suspend written to the device will reset the device back to Read mode. Once the 80 μs window has timed out, only the Erase suspend command is recognized. Note that although the Reset command is not recognized in the Erase Suspend mode, the device is available for read or program operations in sectors that are not erase suspended. The Erase Suspended and Erase Resume commands may be written as often as required during a sector erase operation. Hence, once erase has begun, it must ultimately complete unless Hardware Reset is initiated. Loading the sector erase registers may be done in any sequence and with any number of sectors (0 to 18).

Sector erase does **not** require the user to program the device prior to erase. The device automatically preprograms all memory locations, within sectors to be erased, prior to electrical erase. When erasing a sector or sectors, the remaining unselected sectors or the write protected sectors are unaffected. The system is not required to provide any controls or timings during sector erase operations. The Erase Suspend and Erase Resume commands may be written as often as required during a sector erase operation.

Automatic sector erase operations begin on the rising edge of the $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) pulse of the last sector erase command issued, and once the 80 μs time-out window has expired. The status of the sector erase operation can be determined three ways:

- $\overline{\text{DATA}}$ Polling of DQ7
- Checking the status of the toggle bit DQ6
- Checking the status of the RY/ $\overline{\text{BY}}$ pin

Further status of device activity during the sector erase operation can be determined using toggle bits DQ2 and DQ3.

Figure 5 illustrates the Embedded Erase Algorithm, using a typical command sequence and bus operations.

Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data

read or programs in a sector not being erased. This command is applicable **only** during the Sector Erase operation, which includes the time-out period for Sector Erase. The Erase Suspend command will be ignored if written during the execution of the Chip Erase operation or Embedded Program Algorithm (but will reset the chip if written improperly during the command sequences.) Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation. Once in Erase Suspend, the device is available for read (note that in the Erase Suspend mode, the Reset/Read command is not required for read operations and is ignored) or program operations in sectors not being erased. Any other command written during the Erase Suspend mode will be ignored, except for the Erase Resume command. Writing the Erase Resume command resumes the sector erase operation. The addresses are “don’t cares” when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 μ s and 20 μ s to actually suspend the operation and go into erase suspended read mode (pseudo-read mode), at which time the user can read or program from a sector that is **not** erase suspended. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase suspended.

Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ2 to toggle. Polling DQ2 on successive reads from a given sector provides the system the ability to determine if a sector is in Erase Suspend.

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase suspend-program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode, except that the data must be programmed to sectors that are not erase suspended. Successively reading from the erase suspended sector while the device is in the erase suspend-program mode will cause DQ2 to toggle. Completion of the erase suspend operation can be determined two ways:

- Checking the status of the toggle bit DQ2
- Checking the status of the RY/ $\overline{\text{BY}}$ pin

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. However, another Erase Suspend command can be written after the device has resumed sector erase operations.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Write Operation Status

Address Sensitivity of Write Status Flags

Detailed in Table 6 are all the status flags that can be used to check the status of the device for current mode operation. During Sector Erase, the part provides the status flags automatically to the I/O ports. The information on DQ2 is address sensitive. This means that if an address from an erasing sector is consecutively read, then the DQ2 bit will toggle. However, DQ2 will not toggle if an address from a non-erasing sector is consecutively read. This allows the user to determine which sectors are erasing and which are not.

Once Erase Suspend is entered, address sensitivity still applies. If the address of a non-erasing sector (that is, one available for read) is provided, then stored data can be read from the device. If the address of an erasing sector (that is, one unavailable for read) is applied, the device will output its status bits. Confirmation of status bits can be done by doing consecutive reads to toggle DQ2, which is active throughout the Embedded Erase mode, including Erase Suspend.

In order to effectively use $\overline{\text{DATA}}$ Polling to determine if the device has entered into erase-suspended mode, it is necessary to apply a sector address from a sector being erased.

Table 6. Hardware Sequence Flags

		Status	DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY
In Progress	Programming		$\overline{\text{DQ7}}$	Toggle	0	0	No Toggle	0
	Program/Erase in Auto-Erase		0	Toggle	0	1	(Note 1)	0
	Erase Suspend Mode	Erase Sector Address	1	No Toggle	0	0	Toggle (Note 1)	1
		Non-Erase Sector Address	Data	Data	Data	Data	Data (Note 2)	1
	Program in Erase Suspend		$\overline{\text{DQ7}}$ (Note 2)	Toggle	0	0	1 (Note 2)	0
Exceeded Time Limits	Programming		$\overline{\text{DQ7}}$	Toggle	1	0	No Toggle	0
	Program/Erase in Auto-Erase		0	Toggle	1	1	(Note 3)	0
	Program in Erase Suspend		$\overline{\text{DQ7}}$	Toggle	1	0	No Toggle	0

Notes:

1. DQ2 can be toggled when the sector address applied is that of an erasing or erase suspended sector. Conversely, DQ2 cannot be toggled when the sector address applied is that of a non-erasing or non-erase suspended sector. DQ2 is therefore used to determine which sectors are erasing or erase suspended and which are not.
2. These status flags apply when outputs are read from the address of a non-erase-suspended sector.
3. If DQ5 is high (exceeded timing limits), successive reads from a problem sector will cause DQ2 to toggle.

DQ7: $\overline{\text{DATA}}$ Polling

The Am29LV008 features $\overline{\text{DATA}}$ Polling as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the compliment of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. Note that just at the instant when DQ7 switches to true data, the other bits, DQ6–DQ0, may not yet be true data. However, they will all be true data on the next read from the device. **Please note that $\overline{\text{DATA}}$ Polling (DQ7) may give an inaccurate result when an attempt is made to write to a protected sector.** During an Embedded Erase Algorithm, an attempt to read the device will produce a '0' at the DQ7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce a '1' at DQ7.

For chip erase, the $\overline{\text{DATA}}$ Polling is valid (DQ7 = 1) after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{DATA}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. $\overline{\text{DATA}}$ Polling must be performed at sector addresses within any of the sectors being erased and not a sector that is within a protected sector. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations, DQ7 may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the

device is driving status information on DQ7 at one instant of time and in the next instance of time, that byte has valid data. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has valid data, DQ0–DQ6 may still provide write operation status. The valid data on DQ0–DQ7 can be read on the next successive read attempt.

The $\overline{\text{DATA}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, erase suspend-program mode, or sector erase time-out (see Table 6).

If the user attempts to write to a protected sector, $\overline{\text{DATA}}$ Polling will be activated for about 1 μs ; the device will then return to read mode, with data from the protected sector unchanged. If the user attempts to erase a protected sector, Toggle Bit will be activated for about 50 μs ; the device will then return to read mode, without having erased the protected sector.

See Figure 6 for the $\overline{\text{DATA}}$ Polling timing specifications and diagrams.

DQ6: Toggle Bit

The Am29LV008 also features a "Toggle Bit" as a method to indicate to the host system whether the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the

Embedded Program or Erase Algorithm is completed, DQ6 will stop toggling and valid data can be read on the next successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth \overline{WE} pulse in the four-write-pulse sequence. During Chip erase, the Toggle Bit is valid after the rising edge of the sixth \overline{WE} pulse in the six-write-pulse sequence. During Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase \overline{WE} pulse. The Toggle Bit is active during the Sector Erase time-out.

Either \overline{CE} or \overline{OE} toggling will cause DQ6 to toggle. If the user attempts to write to a protected sector, \overline{DATA} Polling will be activated for about 1 μ s; the device will then return to read mode, with data from the protected sector unchanged. If the user attempts to erase a protected sector, Toggle Bit will be activated for about 50 μ s; the device will then return to read mode, without having erased the protected sector.

DQ5: Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions, DQ5 will produce a '1' indicating that the program or erase cycle was not successfully completed. Write operation status and reset command are the only operating functions under this condition. The device will draw active power under this condition.

The DQ5 failure condition will also appear if the user attempts to write a data '1' to a bit that has already been programmed to a data '0'. In this case, the DQ5 failure condition is not guaranteed to happen, since the device was incorrectly used. Please note that programming a data '0' to a data '1' should never be attempted, and only erasure should be used for this purpose. If programming to a data '1' is attempted, the device should be reset.

If the DQ5 failure condition is observed while in Sector Erase mode (that is, exceeded timing limits), then DQ2 can be used to determine which sector had the problem. This is especially useful when multiple sectors have been loaded for erase.

DQ3: Sector Erase Timer

After the completion of the initial Sector Erase command sequence, the Sector Erase time-out will begin. DQ3 will remain low until the time-out is complete. \overline{DATA} Polling (DQ7) and Toggle Bit (DQ6) are also valid after the first sector erase command sequence.

If \overline{DATA} Polling or the Toggle Bit indicates the device has been written with a valid Sector Erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ('1'), the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by the \overline{DATA} Polling or Toggle Bit. If DQ3 is low ('0'), the device will accept additional sector erase commands. To be certain the command has been accepted, the software should check the status of DQ3 following each Sector Erase command. If DQ3 was high on the second status check, the command may not have been accepted.

It is recommended that the user guarantee the time between sector erase command writes be less than 80 μ s by disabling the processor interrupts just for the duration of the Sector Erase (30H) commands. This approach will ensure that sequential sector erase command writes will be written to the device while the sector erase timer window is still open.

DQ2: Toggle Bit 2

This toggle bit, along with DQ6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspend-read mode, successive reads from the erase-suspended sector will cause DQ2 to toggle. When the device is in the erase suspend-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic '1' at the DQ2 bit. Note that a sector which is selected for erase is not available for read in Erase Suspend mode. Other sectors which are not selected for Erase can be read in Erase Suspend.

DQ6 is different from DQ2 in that DQ6 toggles only when the standard program or erase, or erase suspend-program operation is in progress.

If the DQ5 failure condition is observed while in Sector Erase mode (that is, exceeded timing limits), the DQ2 toggle bit can give extra information. In this case, the normal function of DQ2 is modified. If DQ5 is at logic '1', then DQ2 will toggle with consecutive reads only at the sector address that caused the failure condition. DQ2 will toggle at the sector address where the failure occurred and will not toggle at other sector addresses.

RY/BY: Ready/Busy Pin

The Am29LV008 provides a RY/BY open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or have been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/BY pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the Am29LV008 is placed in an Erase

Suspend mode, the RY/BY output will be high. For programming, the RY/BY is valid (RY/BY=0) after the rising edge of the fourth WE pulse in the four write pulse sequence. For chip erase, the RY/BY is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For sector erase, the RY/BY is also valid after the rising edge of the sixth WE pulse.

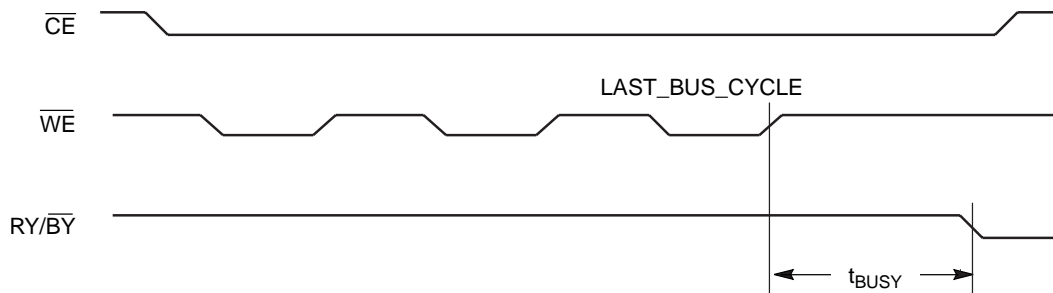
Since the RY/BY pin is an open-drain output, several RY/BY pins can be tied together in parallel with a pull-up resistor to VCC.

Table 7. Toggle Bit Status

Mode	DQ7	DQ6	DQ2
Program	DQ7	Toggles	1
Erase	0	Toggles	Toggles
Erase-Suspend Read (Note 1) (Erase-Suspended Sector)	1	1	Toggles
Erase Suspend Program	DQ7 (Note 2)	Toggles	1 (Note 2)

Notes:

1. These status flags apply when outputs are read from a sector that has been erase suspended.
2. These status flags apply when outputs are read from the addresses of the non-erase suspended sector.



20511C-4

Figure 1. RY/BY Timing Diagram

RESET: Hardware Reset Pin

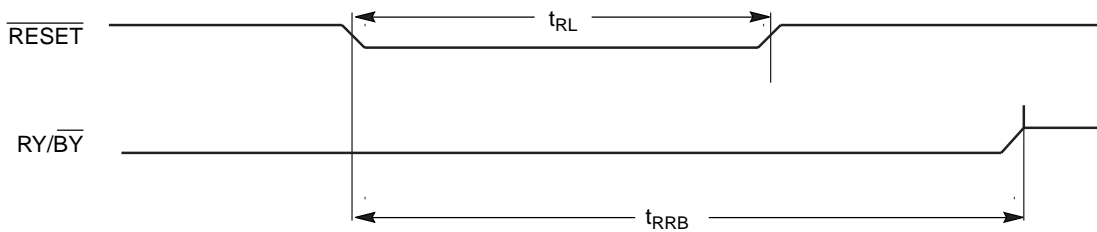
The $\overline{\text{RESET}}$ pin is an active low signal. A logic '0' on this pin will force the device out of any mode that is currently executing back to the reset state. This allows a system reset to take effect immediately without having to wait for the device to finish a long execution cycle. To avoid a potential bus contention during a system reset, the device is isolated from the data I/O bus by tri-stating the data output pins for the duration of the $\overline{\text{RESET}}$ pulse.

If $\overline{\text{RESET}}$ is asserted during a program or erase operation, the RY/ $\overline{\text{BY}}$ pin will remain low until the reset operation is internally complete. This will require between 1 μs and 20 μs . Hence the RY/ $\overline{\text{BY}}$ pin can be used to signal that the reset operation is complete. Otherwise, allow for the maximum reset time of 20 μs . If $\overline{\text{RESET}}$ is asserted when a program or erase operation is not ex-

ecuting (RY/ $\overline{\text{BY}}$ pin is high), the reset operation will be complete within 500 ns.

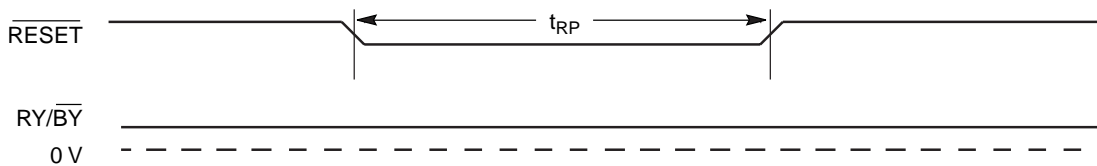
Asserting $\overline{\text{RESET}}$ during a program or erase operation leaves erroneous data stored in the address locations being operated on at the time of device reset. These locations need updating after the reset operation is complete. See Figure 2 for timing specifications.

The device enters I_{CC4} standby mode (200 nA) when $V_{\text{SS}} \pm 0.3 \text{ V}$ is applied to the $\overline{\text{RESET}}$ pin. The device can enter this mode at any time, regardless of the logical condition of the $\overline{\text{CE}}$ pin. Furthermore, entering I_{CC4} during a program or erase operation leaves erroneous data in the address locations being operated on at the time of the $\overline{\text{RESET}}$ pulse. These locations need updating after the device resumes standard operations. After the $\overline{\text{RESET}}$ pin goes high, a minimum latency period of 50 ns must occur before a valid read can take place.



20511C-5

Figure 2. Device Reset During a Program or Erase Operation



20511C-6

Figure 3. Device Reset During Read Mode

Data Protection

The Am29LV008 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power-up, the device automatically resets the internal state machine to the read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of the command sequences.

The Am29LV008 incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (lock-out voltage). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO} . It is the user's responsibility to ensure that the control levels are logically correct when V_{CC} is above V_{LKO} (unless the RESET pin is asserted).

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on \overline{OE} , \overline{CE} , or \overline{WE} will not change the command registers.

Logical Inhibit

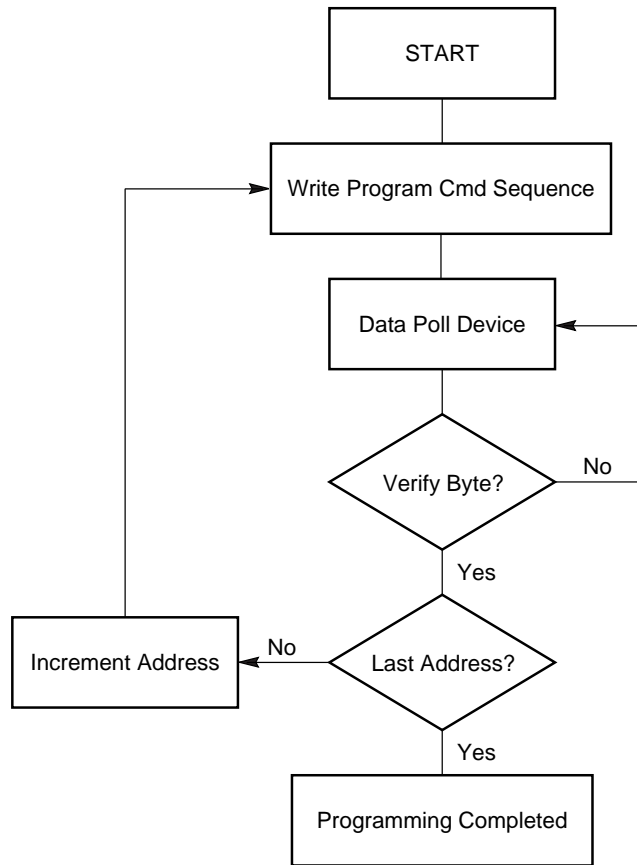
Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write, \overline{CE} and \overline{WE} must be logical zero while \overline{OE} is a logical one.

Power-Up Write Inhibit

Power up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of \overline{WE} . The internal state machine is automatically reset to read mode on power up.

EMBEDDED ALGORITHMS
Embedded Program Algorithm

3.0 V-only Flash



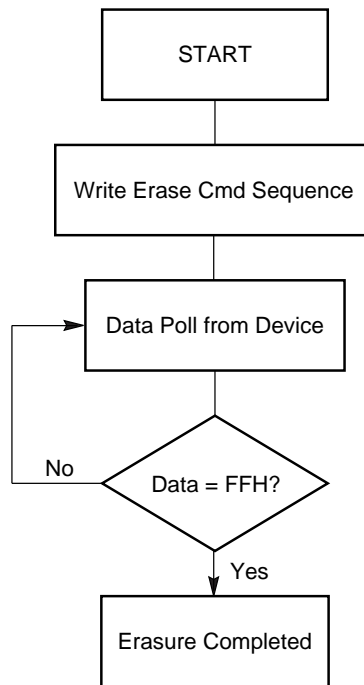
20511C-7

Figure 4. Embedded Program Algorithm

Bus Operation	Command Sequence	Comments
Standby*		
Write	Program	Valid Address/Data
Read		DATA Polling to Verify Programming
Standby*		Compare Data Output to Data Expected

* Device is either powered-down, erase inhibit, or program inhibit.

Embedded Erase Algorithm

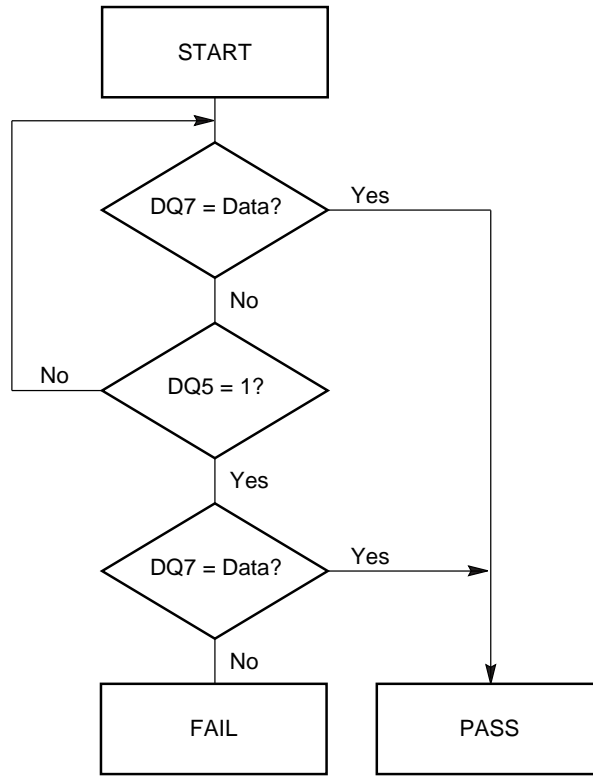


20511C-8

Figure 5. Embedded Erase Algorithm

Bus Operation	Command Sequence	Comments
Standby		
Write	Erase	
Read		$\overline{\text{DATA}}$ Polling to Verify Erasure
Standby		Compare Output to FFH

Data Polling Algorithm

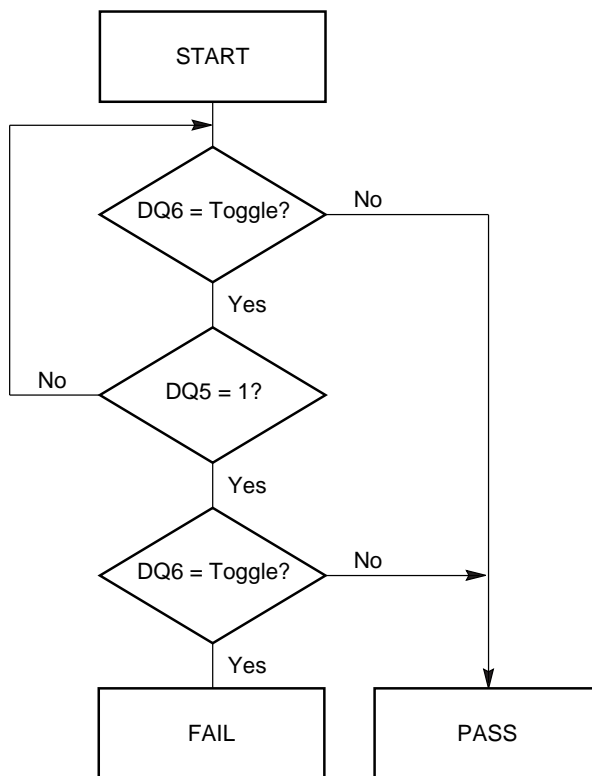


3.0 V-only Flash

20511C-9

Figure 6. Data Polling Algorithm

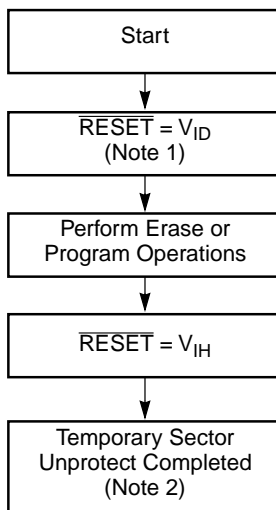
Toggle Bit Algorithm



20511C-10

Figure 7. Toggle Bit Algorithm

Temporary Sector Unprotect Algorithm



Notes:

- 1. All protected sectors unprotected.
- 2. All previously protected sectors are protected once again.

20511C-11

Figure 8. Temporary Sector Unprotect Algorithm

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Plastic Packages	-65°C to +150°C
Ambient Temperature	
with Power Applied	-55°C to +125°C
Voltage with Respect to Ground	
All pins except A9, \overline{OE} and \overline{RESET}	
(Note 1)	-0.5 V to $V_{CC}+0.5$ V
V_{CC} (Note 1)	-0.5 V to +3.6 V
A9, \overline{OE} , and \overline{RESET} (Note 2)	-0.5 V to +13.0 V
Output Short Circuit Current (Note 3)	200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC} + 0.5$ V. During voltage transitions, input or I/O pins may overshoot to $V_{CC} + 2.0$ V for periods up to 20 ns. See Tables 10 and 11.
2. Minimum DC input voltage on pins A9, \overline{OE} , and \overline{RESET} is -0.5 V. During voltage transitions, A9, \overline{OE} , and \overline{RESET} may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns. See Tables 10 and 11.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A) 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) -40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) -55°C to +125°C

 V_{CC} Supply Voltages

V_{CC} for Am29LV008T/B-90R +3.0 V to 3.6 V

V_{CC} for Am29LV008T/B-100,
-120, -150 +2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

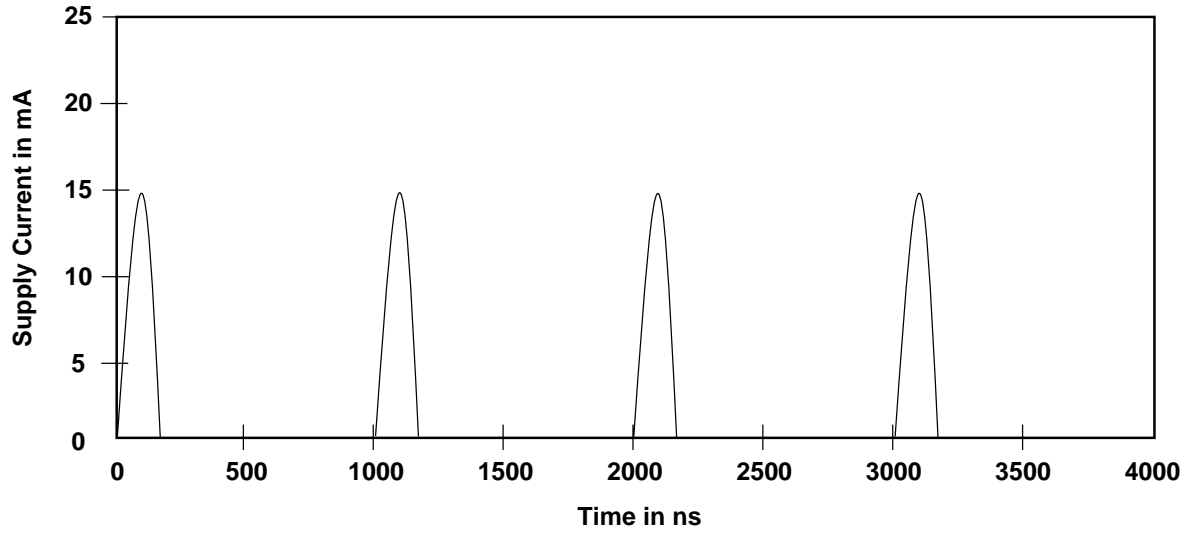
Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC\ max}$		± 1.0	μA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 13.0 V		35	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC\ max}$		± 1.0	μA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ at 5 MHz		16	mA
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ at 1 MHz		4	mA
I_{CC2}	V_{CC} Active Current (Notes 1, 2, and 4)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC\ max}$; \overline{CE} , $\overline{RESET} = V_{CC} \pm 0.3\ V$		5	μA
I_{CC4}	V_{CC} Standby Current During Reset	$V_{CC} = V_{CC\ max}$; $\overline{CE} = V_{CC} \pm 0.3\ V$; $\overline{RESET} = V_{SS} \pm 0.3\ V$		5	μA
I_{CC5}	Automatic Sleep Mode (Note 3)	$V_{IH} = V_{CC} \pm 0.3\ V$; $V_{IL} = V_{SS} \pm 0.3\ V$		5	μA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		$0.7 \times V_{CC}$	$V_{CC} + 0.3$	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	$V_{CC} = 3.3\ V$	11.5	12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 4.0\ mA$, $V_{CC} = V_{CC\ min}$		0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.0\ mA$, $V_{CC} = V_{CC\ min}$	$0.85 V_{CC}$		V
V_{OH2}		$I_{OH} = -100\ \mu A$, $V_{CC} = V_{CC\ min}$	$V_{CC} - 0.4$		
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)		2.3	2.5	V

Notes:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH} .
2. I_{CC} active while Embedded Erase or Embedded Program is in progress.
3. Automatic sleep mode enables the low power mode when addresses remain stable for 200 ns. Typical sleep mode current is 200 nA.
4. Not 100% tested.

DC CHARACTERISTICS (CONTINUED)

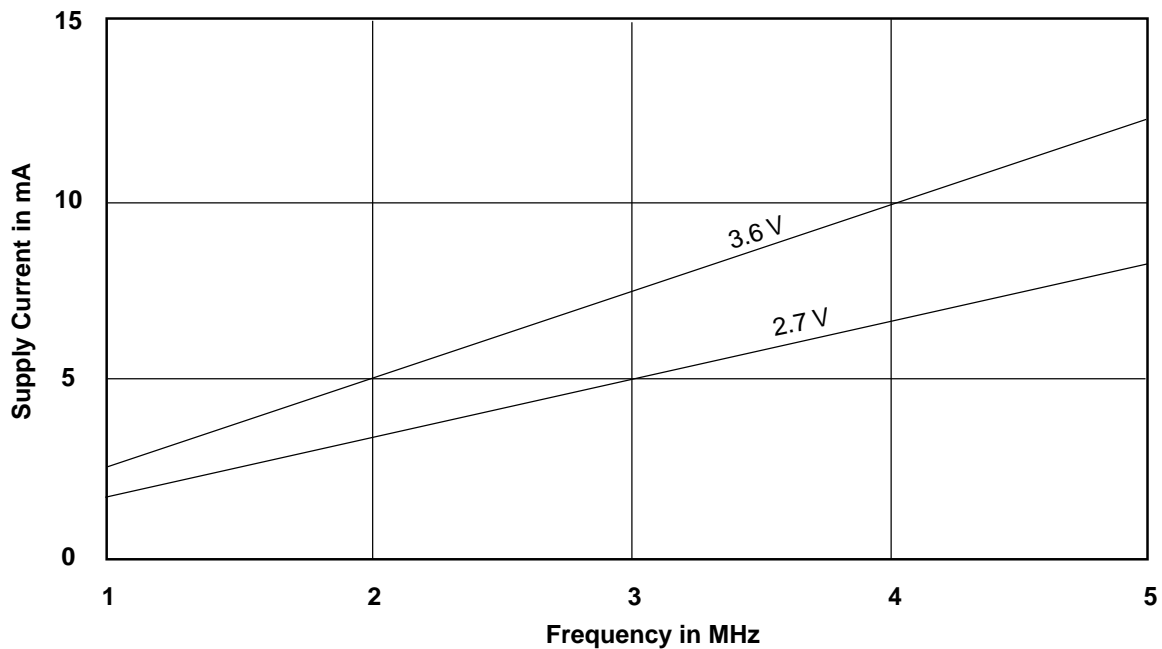
3.0 V-only Flash



Note: Addresses are switching at 1 MHz

20511C-11A

Figure 8A. I_{CC} Current vs. Time



Note: $T = 25^{\circ}C$

20511C-11B

Figure 8B. I_{CC} vs. Frequency

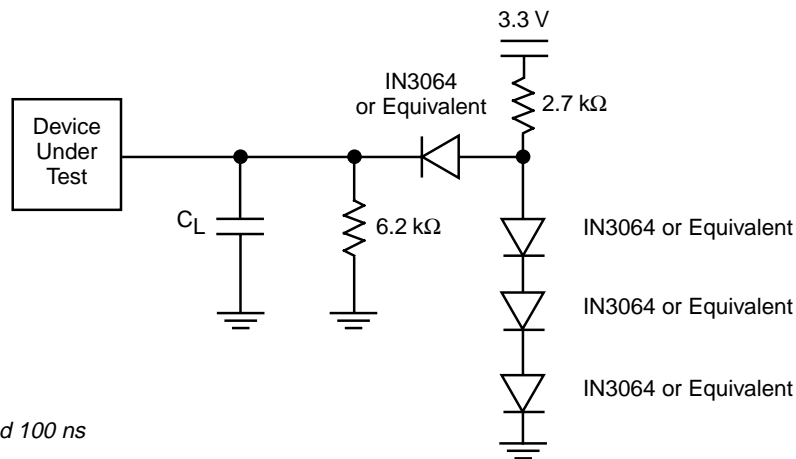
AC CHARACTERISTICS

Read-Only Operations Characteristics

Parameter Symbols		Description	Test Setup	Speed Option (Note 1)				Unit
JEDEC	Standard			-90R	-100	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)	Min	90	100	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$ Max	90	100	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$ Max	90	100	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	Max	40	40	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 2, 3)	Max	30	30	30	40	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 2, 3)	Max	30	30	30	40	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, \overline{CE} or \overline{OE} , Whichever Occurs First (Note 3)	Min	0	0	0	0	ns
	t_{Ready}	RESET Pin Low to Read Mode (Note 3)	Max	20	20	20	20	μ s

Notes:

- Test Conditions
 Input Rise and Fall Times: 5 ns
 Input Pulse Levels: 0.0 V to 3.0 V
 Timing Measurement Reference Level:
 Input: 1.5 V
 Output: 1.5 V
- Output Driver Disable Time
- Not 100% tested.



Notes:

- $C_L = 30$ pF for 90 and 100 ns
- $C_L = 100$ pF for 120 and 150 ns

20511C-12

Figure 9. Test Conditions

AC CHARACTERISTICS

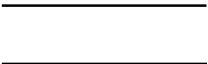
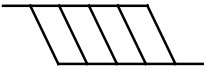
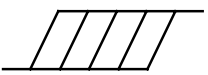
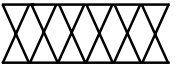
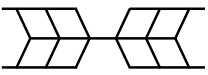
Write (Erase/Program) Operations

Parameter Symbols		Description						Unit
JEDEC	Standard							
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)	Min	90	100	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	50	50	50	65	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	50	50	50	65	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (Note 2)	Min	0	0	0	0	ns
	t_{OEHL}	Output Enable Hold Time	Min	0	0	0	0	ns
		Read (Note 2) Toggle and Data Polling (Note 2)	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (\overline{OE} High to \overline{WE} Low)	Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	\overline{CE} Setup Time	Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	\overline{CE} Hold Time	Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	50	50	50	65	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	30	30	35	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Typ	9	9	9	9	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ	1	1	1	1	sec
	t_{VCS}	V_{CC} Setup Time	Min	50	50	50	50	μ s
	t_{RB}	Write Recovery Time from $R\overline{Y}/\overline{B\overline{Y}}$	Min	0	0	0	0	ns
	t_{RH}	\overline{RESET} High Time Before Read	Min	50	50	50	50	ns
	t_{RPD}	\overline{RESET} To Power Down Time	Min	20	20	20	20	μ s
	t_{BUSY}	Program/Erase Valid to $R\overline{Y}/\overline{B\overline{Y}}$ Delay	Min	90	90	90	90	ns
	t_{VIDR}	Rise Time to V_{ID}	Min	500	500	500	500	ns
	t_{RP}	\overline{RESET} Pulse Width	Min	500	500	500	500	ns
	t_{RRB}	\overline{RESET} Low to $R\overline{Y}/\overline{B\overline{Y}}$ High	Max	20	20	20	20	μ s
	t_{RSP}	\overline{RESET} Setup Time for Temporary Sector Unprotect	Min	4	4	4	4	μ s

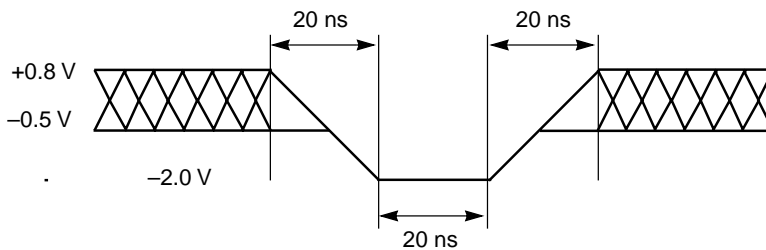
Notes:

1. The duration of the program or erase operation is variable and is calculated in the internal algorithms.
2. Note 100% tested.

KEY TO SWITCHING WAVEFORMS

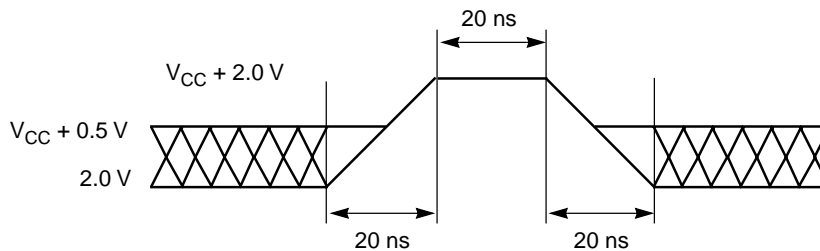
WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL



20511C-13

Figure 10. Maximum Negative Overshoot Waveform

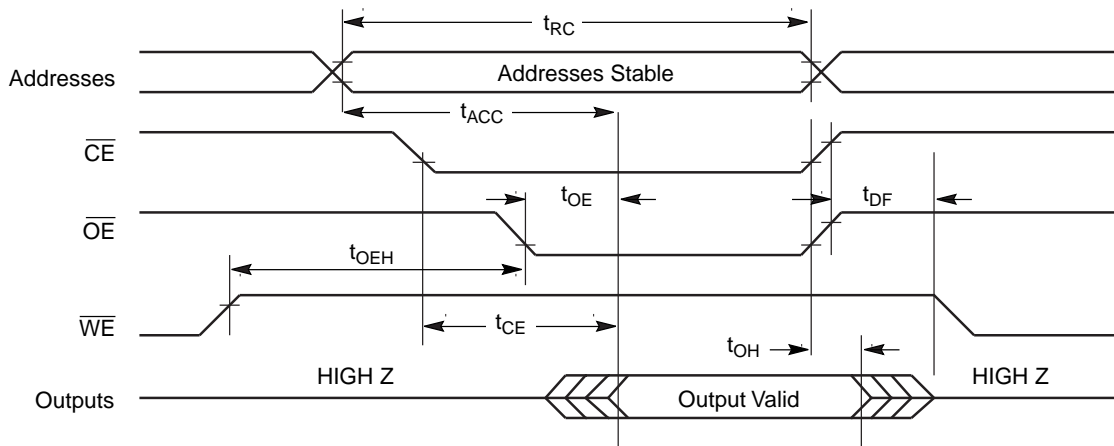


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Figure 11. Maximum Positive Overshoot Waveform

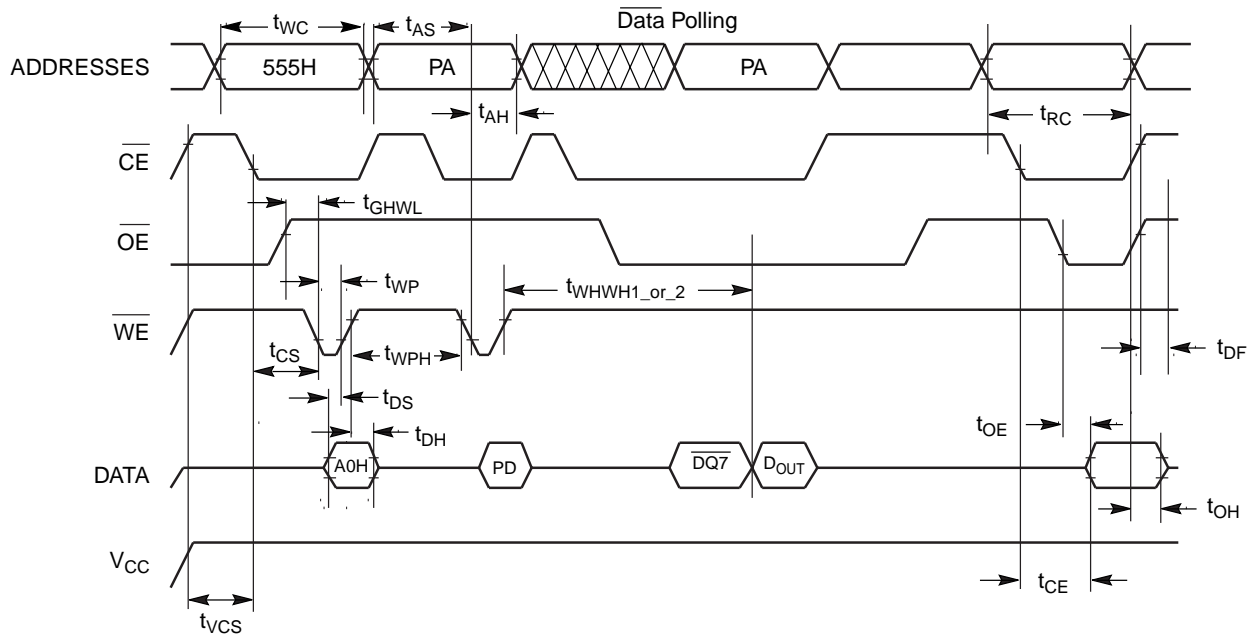
SWITCHING WAVEFORMS

3.0 V-only Flash



20511C-15

Figure 12. AC Waveforms for Read Operations



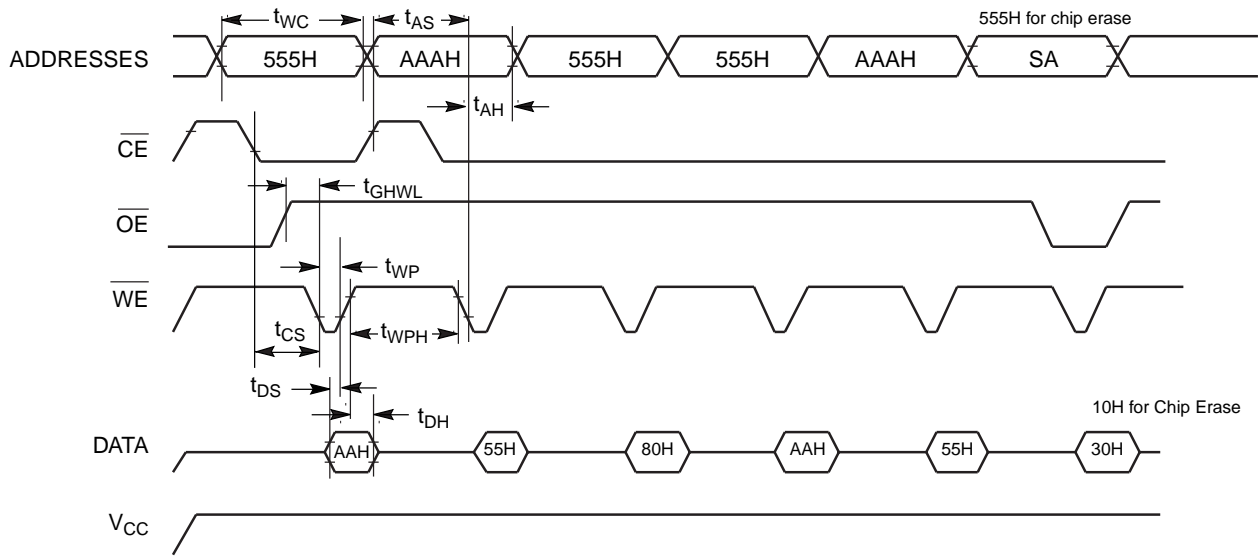
Notes:

1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. D_{OUT} is the output of the data written to the device.
3. PA is the address of the memory location to be programmed.
4. PD is the data to be programmed at the byte address.
5. Illustration shows the last two cycles of a four-bus-cycle sequence.

20511C-16

Figure 13. AC Waveforms for Program Operations

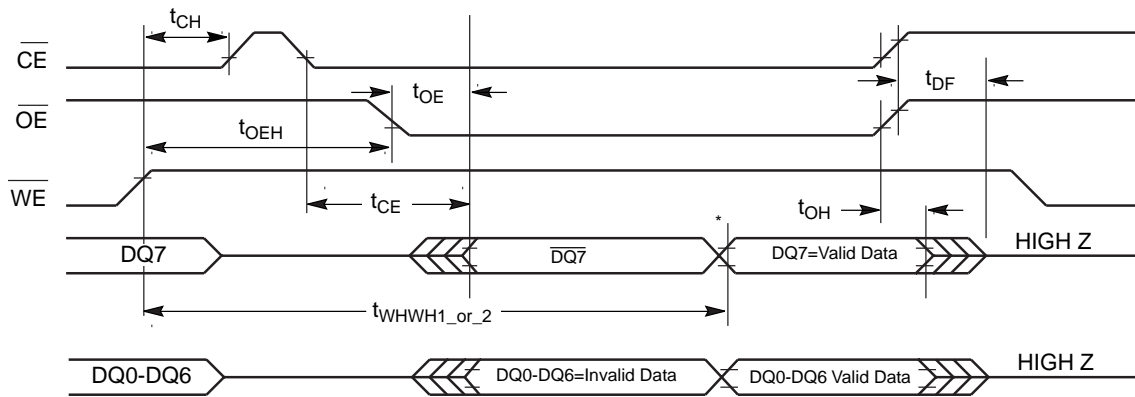
SWITCHING WAVEFORMS



Note:
1. SA is the sector address for Sector Erase.

20511C-17

Figure 14. AC Waveforms for Chip/Sector Erase Operations

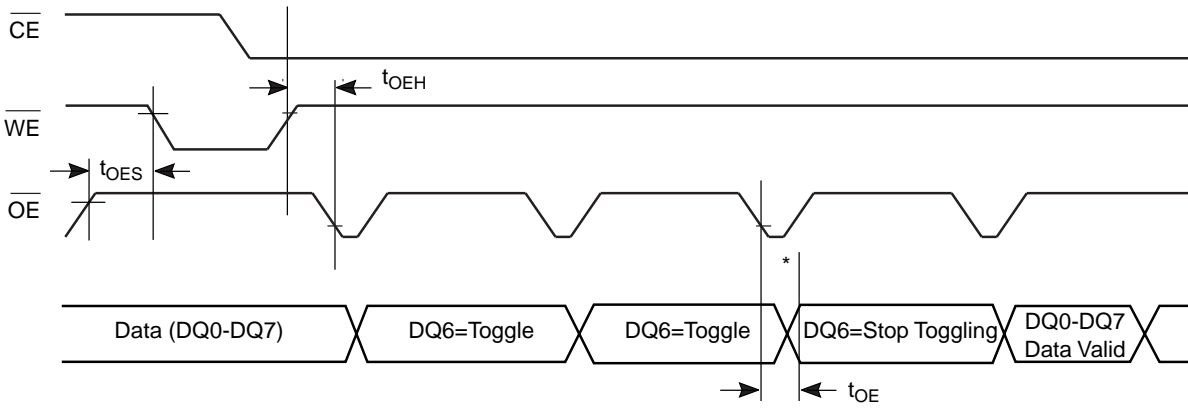


* DQ7 = Valid Data (The device has completed the embedded operation.)

20511C-18

Figure 15. AC Waveforms for Data Polling During Embedded Algorithm Operations

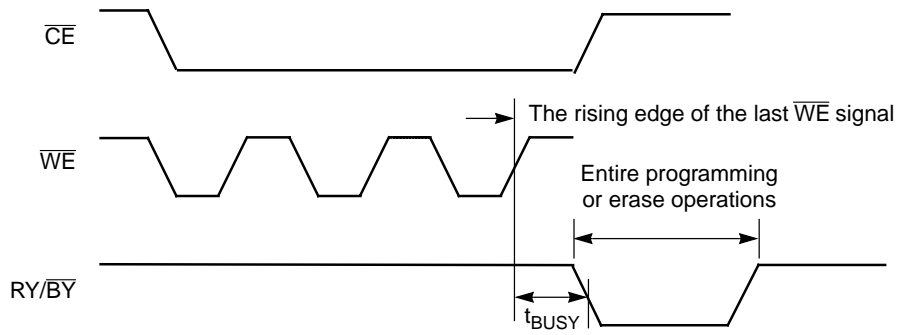
SWITCHING WAVEFORMS



DQ6 stops toggling (The device has completed the embedded operation.)

20511C-19

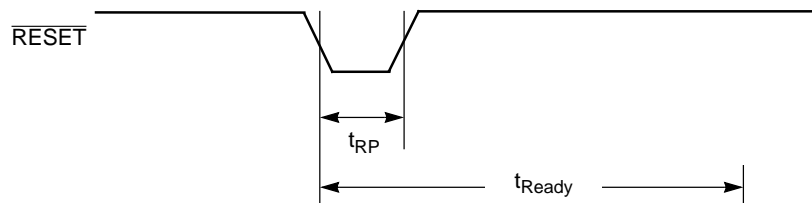
Figure 16. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



DQ7 = Valid Data (The device has completed the embedded operation.)

20511C-20

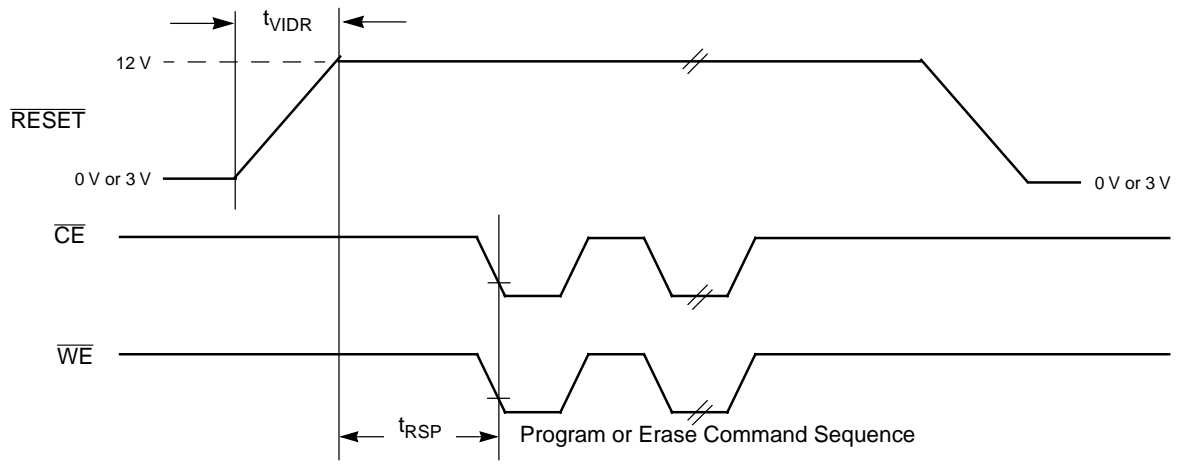
Figure 17. RY/BY Timing Diagram During Program/Erase Operations



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Figure 18. RESET Timing Diagram

SWITCHING WAVEFORMS



20511C-22

Figure 19. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS

Write (Erase/Program) Operations

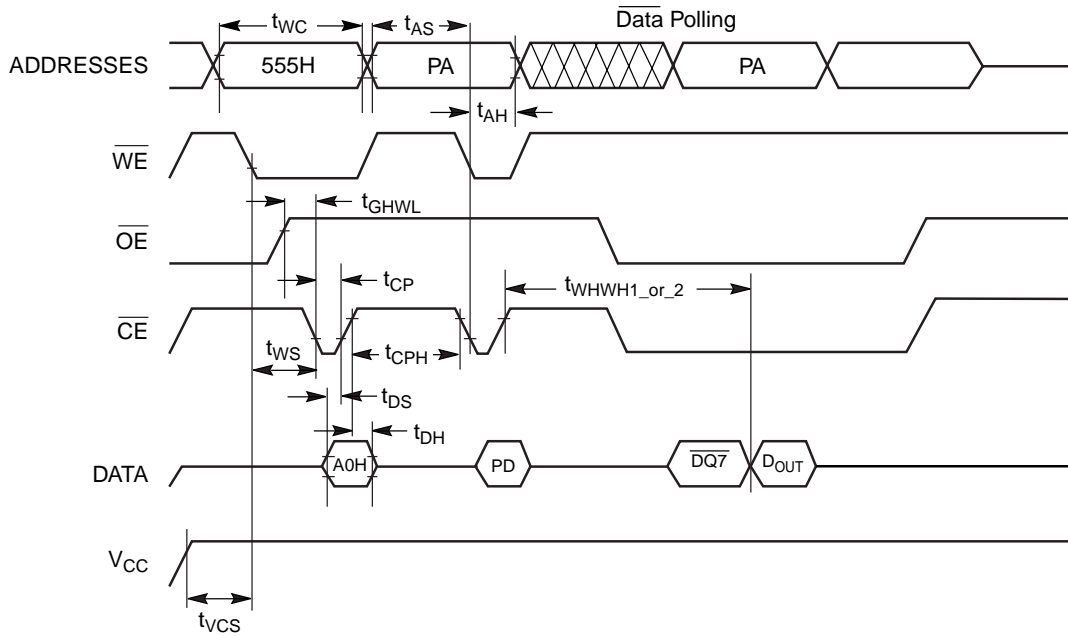
Alternate \overline{CE} Controlled Writes

Parameter Symbols		Description						Unit
JEDEC	Standard							
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	100	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	50	50	50	65	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	50	50	50	65	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Min	0	0	0	0	ns
		Read (Note 1) Toggle and \overline{Data} Polling (Note 1)	Min	10	10	10	10	ns
t_{GHLEL}	t_{GHLEL}	Read Recovery Time Before Write (\overline{OE} High to \overline{WE} Low)	Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	\overline{WE} Setup Time	Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	\overline{WE} Hold Time	Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	\overline{CE} Pulse Width	Min	50	50	50	65	ns
t_{EHEL}	t_{CPH}	\overline{CE} Pulse Width High	Min	30	30	30	35	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Typ	9	9	9	9	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 3)	Typ	1	1	1	1	sec

Notes:

1. Not 100% tested.
2. The duration of the program or erase operation is variable and is calculated in the internal algorithms.
3. Does not include the preprogramming time.

SWITCHING WAVEFORMS



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ7}$ is the complement of the data written to the device.
4. D_{OUT} is the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

20511C-23

Figure 20. Alternate \overline{CE} Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 2)	Max (Note 3)	Unit	Comments
Sector Erase Time	1	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	19		s	
Byte Programming Time	9	300	μ s	Excludes system level overhead (Note 5)
Chip Programming Time	9	27	s	
Erase/Program Endurance	1,000,000		cycles	Minimum 100,000 cycles guaranteed

Notes:

1. The typical program and erase times are considerably less than the maximum times since most bytes program or erase significantly faster than the worst case byte. The device enters the failure mode (DQ5="1") only after the maximum times given are exceeded. See the section on DQ5 for further information.
2. Except for erase and program endurance, the typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC} , 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.
3. Under worst case conditions of 90°C, $V_{CC} = 2.7$ V, 100,000 cycles.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the four-bus-cycle sequence for the program command. See Table 5 for further information on command definitions.

LATCHUP CHARACTERISTICS

	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE, and RESET)	-1.0 V	13.0 V
Input voltage with respect to V_{SS} on all I/O pins	-1.0 V	$V_{CC} + 1.0$ V
V_{CC} Current	-100 mA	+100 mA

Includes all pins except V_{CC} . Test conditions: $V_{CC} = 3.0$ V, one pin at a time.

TSOP PIN CAPACITANCE (Notes 1–2)

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz.

DATA SHEET REVISION SUMMARY FOR AM29LV008

Distinctive Characteristics:

Rearranged bullets. Renamed “2.7 to 3.6 volt, extended voltage range...” to “Single power supply operation.” Under “Single power supply operation” and “High performance” bullets, defined standard and extended voltage ranges and added 90 ns speed option. Combined “Advanced power management” and “Low current consumption” bullets into new “Ultra low power consumption” bullet. Under that bullet, revised the typical standby and automatic sleep mode current specifications from 1 μ A to 200 nA; revised read current specification from 10 mA to 2 mA/MHz. Combined “Sector protection” and “Flexible sector architecture” bullets. Under flexible sector architecture bullet, added temporary sector unprotect feature description. Combined Embedded Program and Embedded Erase bullets under new “Embedded Algorithms” bullet; removed TM designations. Clarified descriptions of sector protection, erase suspend/resume, hardware reset pin, ready/busy pin, and data polling and toggle bits.

General Description:

Added text on new speed option and voltage range to the second paragraph.

Product Selector Guide:

Added -90R voltage range and speed option.

Pin Configuration:

Added new voltage range for -90R to V_{CC} specification.

Ordering Information, Standard Products:

The -90R speed option is now listed in the example. Revised “Speed Option” section to indicate both voltage ranges.

Valid Combinations: Added -90R speed option and voltage range.

Automatic Sleep Mode:

Revised addresses stable time to 200 ns and current draw to 200 nA.

Table 5, Command Definitions:

Grouped address designators PA, PD, RA, RD, and SA under the legend heading. Modified SA definition to accommodate the sector protect verify command. Since unlock addresses only require address bits A0–A10 to be valid, the number of hexadecimal digits in the unlock addresses were changed from four to three. The remaining upper address bits are don't care. Removed “H” designation from hexadecimal values in table and replaced with new Note 1. Revised Notes 5 and 6 to indicate when commands are valid; are now new Notes 4 and 5. Expanded autoselect section to show each function separately: manufacturer ID, device ID, and

sector protect verify. Added note 3 to explain sector protect codes. In Note 8, changed A13 to A11, added “unless otherwise noted”; is now new Note 6.

RESET: Hardware Reset Pin:

Fourth paragraph: Revised standby mode specification to 200 nA.

Operating Ranges:

V_{CC} Supply Voltages: Added 3.0 to 3.6 V voltage range and -90R speed option.

DC Characteristics:

CMOS Compatible: Changed I_{CC1} from 30 mA maximum at 6 MHz to 16 mA maximum at 5 MHz and 4 mA maximum at 1 MHz. Changed I_{CC2} from 35 mA to 30 mA maximum. In the V_{OL} specification, changed the I_{OL} test condition from 5.8 to 4.0 mA. In Note 1, changed 6 MHz to 5 MHz. In Note 3, changed address stable time from 300 ns to 200 ns; changed typical automatic sleep mode current from 1 μ A to 200 nA.

Figure 8A, I_{CC} Current vs. Time, and Figure 8B, I_{CC} vs. Frequency:

Figure 8A illustrates current draw during the Automatic Sleep Mode after the addresses are stable. Figure 8B shows how frequency affects the current draw curves for both voltage ranges.

AC Characteristics:

Read Only Operations Characteristics: Added -90R column.

Test Conditions, Figure 9:

Added 90 ns speed to C_L note.

AC Characteristics:

Write/Erase/Program Operations: Added the -90R column.

Figure 13, AC Waveforms for Program Operations:

Changed 5555H to 555H in addresses waveform to match command definitions (Table 5).

Figure 14, AC Waveforms for Chip/Sector Erase Operations:

Changed 5555H to 555H in addresses waveform to match command definitions (Table 5).

Figure 19, Temporary Sector Unprotect Diagram:

Corrected callouts on $\overline{\text{RESET}}$ waveform to “0 V or 3 V”.

AC Characteristics:

Alternate $\overline{\text{CE}}$ Controlled Writes: Added the -90R column. Changed t_{AH} from 45 to 50 ns for -100, from 50 to 65 ns for -150. Changed t_{DS} from 50 to 65 ns for -150. Changed t_{CP} from 45 to 50 ns for -100, from 50 to 65 ns for -150. Changed t_{CPH} from 20 to 30 ns for -100, -120; from 20 to 35 ns for -150.

Figure 20, Alternate $\overline{\text{CE}}$ Controlled Write Operation Timings:

Changed 5555H to 555H in addresses waveform to match command definitions (Table 5).

Erase and Programming Performance:

Added typical chip erase specification. Renamed erase/program cycles specification to erase/program endurance. Corrected to indicate 1,000,000 cycle endurance is typical, not maximum, and that 100,000

cycle endurance is minimum, not typical. Revised Note 1 to include write endurance; moved Note 1 references in table to table head. Consolidated and moved Note 1 and Note 3 references in table to table head. Combined Note 2 and Note 5 into new Note 1, which applies to the entire table; revised to indicate that DQ5=1 after any maximum time. Comments for program and erase now straddle parameter rows. Separated the two sentences in Note 4 into new Notes 4 and 5; added corresponding note references to comment section.